MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2021/2022 (AC 2.0)

EEE1036– DIGITAL LOGIC DESIGN

(ALL)

3 OCTOBER 2022
02:30 p.m. - 04:30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. 1. This Question paper consists of 5 pages with **4 Questions** only.
2. Attempt **ALL FOUR** questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.
4. Please refer to page 5 for the Appendix.

QUESTION 1

(a) Describe the main difference between digital and analog signals. Give **ONE(1)** example for each of the digital and analog systems. [6 marks]

(b) Refer to **Appendix Q1**, convert the given codes in **Table Q1(a)** to other representations listed and determine the character strings encoded by the ASCII code. Show all the working steps clearly. [7 marks]

Table Q1(a)

Binary Code	Gray Code	ASCII Code	Character strings encoded by ASCII
		4F 7A	
	0010000100101111		

(c) Given two decimal numbers of A=19 and B=47, perform the following two operations: **(–A+B)** and **(–A–B)**, respectively, in 8-bit two's complement system. Check your results by converting the binary result back to decimal.

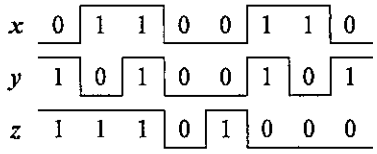
[12 marks]

QUESTION 2

(a) Given the following Boolean expression:

$$F(x, y, z) = \overline{(\bar{x} + y\bar{z}) \bullet (x + z)}$$

(i) Convert the expression into canonical Sum of Products (SOP) form. [7 marks]
(ii) Based on the SOP expression, construct the truth table. [6 marks]
(iii) Draw the output waveform F for the inputs (x, y, z) timing diagram as shown below. [2 mark]



(b) Find the minimum Product of Sums (POS) form of the following function using the Karnaugh-map (K-map).

[10 marks]

$$F(A, B, C, D) = \Pi_M (0, 1, 2, 5, 7, 8, 9, 11, 13) + d (4, 12, 14, 15)$$

Continued...

QUESTION 3

(a) With reference to the logic circuit in **Figure 3.1** and based on your knowledge of the NOR gate, fill up the truth table of the circuit in **Table3.1**. Assume initially Q=1 and Q'=0. Explain with reason if S=1 and R=1 are valid inputs.

[6 marks]

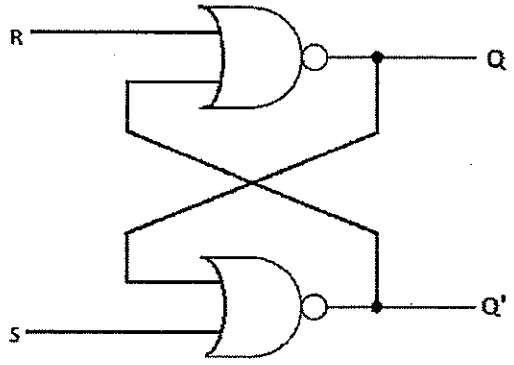


Figure 3.1: SR Latch

Table 3.1

S	R	Q	Q'
0	0		
0	1		
1	0		
1	1		

(b) Modify the SR latch logic circuit in **Figure 3.1** to be a level-triggered SR flip-flop where the flip-flop is triggered by a clock signal EN. [4 marks]

(c) Draw the timing diagram for Q if the S and R signals are given in the **Figure 3.2** below.

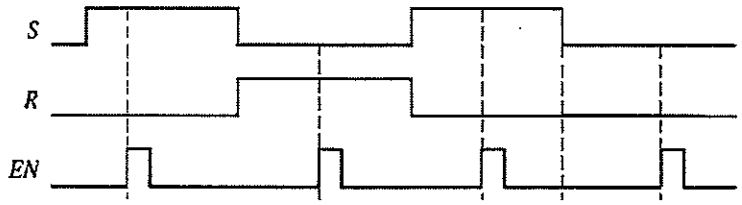


Figure 3.2

[4 marks]

Continued...

(d) The logic circuit in **Figure 3.3** is composed by connecting two T flip-flops. Initially, the state of each flip-flop is reset to 0. The T flip-flop is positive edge-triggered.

(i) Draw the timing diagram to show the output Q0 and Q1 for 4 clock pulses. [4 marks]

(ii) Complete **Table 3.2** to show Q1 and Q0 values for each clock pulse. [4 marks]

(iii) Briefly discuss the function of this circuit. [3 marks]

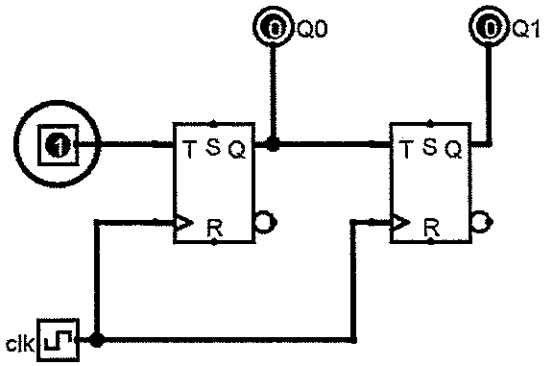


Figure 3.3

Table 3.2

Clock pulse	Q1	Q0
0	0	0
1		
2		
3		
4		

QUESTION 4

(a) Realize the following function $F1$ and $F2$ with the use of a single 3 to 8 decoder and standard logic gates. The number of logic gates must be minimized, and each gate can only accept 2 inputs. The decoder is using active high output. Show all the relevant derivation steps and draw the logic circuit block diagram.

$$F1 = f(x_2, x_1, x_0) = \sum m(2,4)$$

$$F2 = f(x_2, x_1, x_0) = \sum m(4,5,6)$$

[4 marks]

(b) With reference to **Question 4(a)**, implement $F1$ and $F2$ by assuming an active low output for the decoder. Show all the relevant derivation steps and draw the logic circuit block diagram. [8 marks]

Continued...

(c) **Design** a 1-bit full adder with the use of 3-to-8 decoder with active high outputs. Then, show the complete **truth table**. **Draw** the logic circuit block diagram of 1-bit full adder. With the use of the block diagram that represent the 1-bit full adder, **design** a 4-bit full adder. The diagram of the logic circuit must be shown.

[13 marks]

APPENDIX Q1

00	NUL	10	DLE	20	space	30	0	40	@	50	P	60	`	70	p
01	SOH	11	DC1	21	!	31	1	41	A	51	Q	61	a	71	q
02	STX	12	DC2	22	"	32	2	42	B	52	R	62	b	72	r
03	ETX	13	DC3	23	#	33	3	43	C	53	S	63	c	73	s
04	EOT	14	DC4	24	$	34	4	44	D	54	T	64	d	74	t
05	ENQ	15	NAK	25	%	35	5	45	E	55	U	65	e	75	u
06	ACK	16	SYN	26	&	36	6	46	F	56	V	66	f	76	v
07	BEL	17	ETB	27	'	37	7	47	G	57	W	67	g	77	w
08	BS	18	CAN	28	(	38	8	48	H	58	X	68	h	78	x
09	TAB	19	EM	29	)	39	9	49	I	59	Y	69	i	79	y
0A	LF	1A	SUB	2A	*	3A	:	4A	J	5A	Z	6A	j	7A	z
0B	VT	1B	ESC	2B	+	3B	;	4B	K	5B	[	6B	k	7B	{
0C	FF	1C	FS	2C	,	3C	<	4C	L	5C	\	6C	l	7C	|
0D	CR	1D	GS	2D	-	3D	=	4D	M	5D	]	6D	m	7D	}
0E	SO	1E	RS	2E	.	3E	>	4E	N	5E	^	6E	n	7E	~
0F	SI	1F	US	2F	/	3F	?	4F	O	5F	_	6F	o	7F	□

End of Paper